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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/479,375	01/05/2000	Richard E Perego	RA158	2966

7590 01/10/2002

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EXAMINER
VERBRUGGE, KEVIN

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/10/2002

#4

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/479,375	Applicant(s) PEREGO ET AL.	
	Examiner Kevin G Verbrugge	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *1/5/00* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings overcoming the draftsperson's objections will be required when the application is allowed.

Specification

The abstract of the disclosure is objected to because it does not conclude with a period. Correction is required. See MPEP § 608.01(b). Submission of a replacement sheet with the corrected abstract is preferred.

Claim Objections

Claims 23 and 24 are objected to because of the following informalities:

In claim 23, line 11, the second occurrence of "having a" should be deleted to correct a presumed typographical error.

In claim 24, line 2, a period (".") should be added after "subsystems" to correct a presumed typographical error.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12, 14-18, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,977,498 to Rastegar et al., hereinafter simply Rastegar, in view of the admitted prior art (APA) of the specification.

Regarding claims 1, 10, 14, 23, and 24, Rastegar discloses a memory system including the claimed memory controller as memory control box 11 in Fig. 1, described in column 1, lines 42-51 and column 3, line 62 through column 4, line 9. His memory control box includes an interface that includes a plurality of memory subsystem ports.

He shows the claimed first memory subsystem as the leftmost memory module 13.

He shows the claimed plurality of point-to-point (PTP) links as buses 16, each connecting a single memory subsystem port on the memory control box with a single memory module. The claimed first PTP link is shown as the leftmost bus 16, connecting the leftmost memory module 13 to memory control box 11.

Rastegar does not teach that his memory modules include a buffer device having a first and second port, nor does he teach that his memory modules include plural memory devices coupled to the buffer device via the second port.

However, the APA of the specification, pages 2-7 and Figs. 2A, and 2B disclose what was widely known in the art at the time of the invention, namely that memory

modules commonly contained a buffer and plural memory devices connected to that buffer. Specifically, the APA teaches on page 3, line 17 and following, that it was known to use a buffer on a DIMM for address and control signals, as taught in U.S. Patent 5,513,135. Furthermore, on page 4, line 18 and following, the APA teaches that it was known to use a buffer on memory modules for address, control, and data signals, as shown in Figs. 2A and 2B.

Rastegar does not teach that his memory modules include the claimed buffer and plural memory devices, but it would have been obvious to the skilled artisan at the time of the invention to include a buffer and plural memory devices on each of Rastegar's memory modules since such devices were well known at the time of the invention as evidenced by the APA and since using the buffers in the memory modules provides a standard interface for the controller to communicate with, simplifying the controller's duties and providing enhanced control of the memory devices on the module as well-known in the art at the time.

Indeed, the Applicants' invention does not appear to be the placement of buffers and plural memory devices on a memory module (since such is shown in their prior art figures and discussed in their specification as APA) but rather the use of PTP links to connect memory modules to a memory controller, an arrangement clearly taught by Rastegar.

Regarding claims 2, 23, and 24, Rastegar does not teach that his device includes the claimed plurality of connectors, each connected to a respective PTP link.

However, in the APA, the Applicants teach that "Memory capacity is commonly upgraded via memory modules or cards featuring a connector/socket interface" (page 2, lines 8-9) and regarding the known system shown in Fig. 1, "A socket and connector interface may be employed which allows each module to be removed and replaced by a memory module that is faster or includes a higher capacity" (page 3, lines 9-11).

It would have been obvious to the skilled artisan to include the claimed plurality of connectors in Rastegar's device to facilitate adding and removing memory modules from his system.

Regarding claims 3 and 11, Rastegar does not explicitly teach that each of his memory modules is disposed on a respective substrate, but it would have been obvious to the skilled artisan to implement each memory module on a separate substrate so it could be removed and replaced independently of all other memory modules. Typically, each memory module had its own substrate and its own connector for connecting the substrate to the bus. One common implementation of this standard technology is shown in U.S. Patent 5,513,135, cited by the Applicants.

Regarding claim 4, Rastegar does not teach that his PTP links, first memory module, and memory control box include a common substrate. However, it was well within the skill of the ordinary artisan to place any number of electronic components on the same substrate and would have been obvious to do so in order to minimize system

malfunctions due to improper connections between elements on different substrates, for example.

Regarding claims 5, 10, 15, and 16, the claimed plurality of channels and memory device select lines are present in the APA memory subsystem devices.

Regarding claims 6, 12, and 17, the APA contains the claimed plurality of terminated signal lines.

Regarding claims 7 and 18, the APA contains the claimed clock generator and/or clock alignment circuit as the PLL device disclosed on page 4, line 5 and following.

Regarding claims 8 and 9, the APA contains sideband signals as claimed.

Claims 13 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,977,498 to Rastegar et al., hereinafter simply Rastegar, in view of the admitted prior art (APA) of the specification, further in view of the presentation by John Poulton, Signaling in High Performance Memory Systems, IEEE Solid State Circuits Conference, slides 1-59, 2/1999.

Regarding claim 13, Rastegar does not teach the claimed "chaining" technique where a buffer device is coupled to another buffer device using a PTP link.

Poulton discloses such a chaining technique in his slide 57 where he shows a future memory interconnect diagram having memory modules chained together.

It would have been obvious to the skilled artisan to chain memory devices together to achieve additional bandwidth in view of Poulton's clear teaching of such a technique to achieve additional bandwidth.

Regarding claims 19 and 21, Rastegar does not disclose the claimed repeater devices and repeater links since his device includes only four memory modules, each with its own PTP link to the memory control box.

Poulton clearly teaches that "Trees and other networks [are] clearly feasible!" in slide 57 of his presentation, indicating that branching networks may be used for increased bandwidth.

It would have been obvious to one skilled in the art at the time of the invention to implement tree networks in Rastegar's device to increase bandwidth because Poulton teaches that tree networks are clearly feasible. And the simplest tree network possible is that claimed by Applicants, namely a repeater device with plural "branches" or repeater links extending out from it.

Rastegar's device would be modified by placing additional memory modules branching off the modules shown in Fig. 1, where each existing module 13 would have at least two modules attached to it.

Regarding claim 20, Rastegar does not explicitly teach that each of his memory modules is disposed on a respective substrate, but it would have been obvious to the skilled artisan to implement each memory module on a separate substrate so it could be removed and replaced independently of all other memory modules. Typically, each memory module had its own substrate and its own connector for connecting the substrate to the bus. One common implementation of this standard technology is shown in U.S. Patent 5,513,135, cited by the Applicants.

Regarding claim 22, the APA contains the claimed clock generator and/or clock alignment circuit as the PLL device disclosed on page 4, line 5 and following.

Conclusion

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Primary Examiner Kevin Verbrugge by phone at (703) 308-6663.

Any response to this action should be mailed to Commissioner for Patents, Washington, D.C. 20231 or faxed to

(703) 746-7238 After-final
(703) 746-7239 Official
(703) 746-7240 Non-Official/Draft

and labeled appropriately (After-final, Official, Non-Official/Draft). Hand-delivered responses should be brought to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor (Receptionist).

Kevin Verbrugge
Primary Examiner
1/8/02

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IMPORTANT NOTICE

The Examiner's art unit number has changed from 2185 to 2187 due to the recent realignment of TC 2100. Please use the new art unit number of 2187 on all correspondence related to this case.

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